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Approaches to investigate complex grid scenarios by means of novel PHIL methods'

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IEEE PES ISGT Innovative Smart Grid Technologies;
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- Intro
- Topologies of LV Grids
- Interfacing Algorithms for PHIL
- Complex Real-Time System Approach
- Conclusions - Outlook

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Introduction

This work is a motivated by real problems arising from industry projects and on-going cooperation with PV inverter manufacturer as well as distribution network operators (DNOs) on a national and international level.

Target: Determination / enactment to integrate more renewable energy strategies from a technological, economical and not least political point of view.

Various scenarios are of interest and underlie certain applicable safety and quality standards, respectively (LV, MV).

- Safety standards: DIN VDE V 0124-100 (LV), FGW TR3 Rev. 23 (MV)
- Quality standards: VDE-AR-N4105:2011-08 (LV), FGW TR3 Rev. 22 (MV)

Profound knowledge and actual discussions in optimization or prototyping projects of PV inverters referred to state-of-the-art problems are adducted for an expanding range of application of possible PHIL tests .

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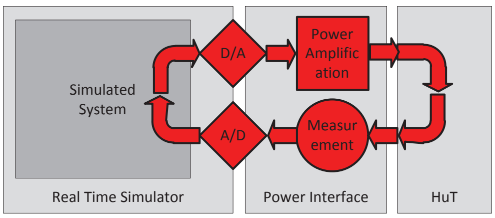
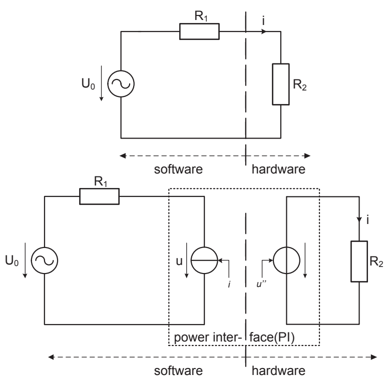
Topologies of LV Grids



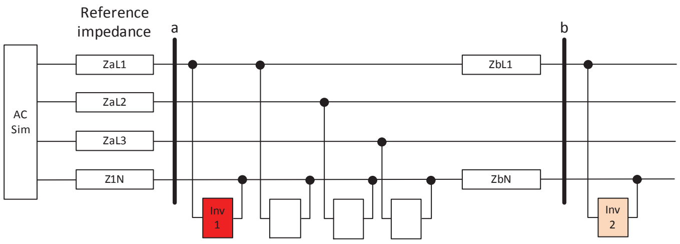


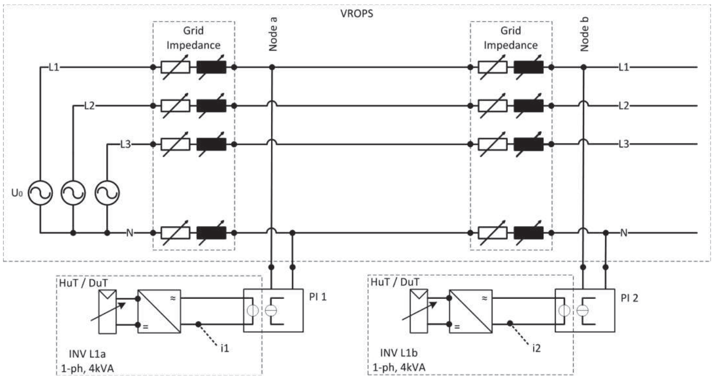
Simple test setup for a PHIL simulation – including dedicated Power interface (PI)

The implementation of PHIL tests environment enforces the use of a dedicated power amplifation units (PA).

- Inherent 'closed-loop originality' of PHIL simulation characterised by:
  - Time delay introduced by real-time system (RTS)
  - Dynamic behaviour of the PA
  - Choice of interface algorithm (IA)
  - Measurement equipment used (I/O, transducers)
- Consequences:
  - Stability considerations (Nyquist criterion)
  - Choice of IA (accuracy, stability, …)
  - Choice of PA (availability, use case, costs, …)
- Power Interfaces (PIs) have to chosen according to the application in PHIL

Topologies of LV Grids





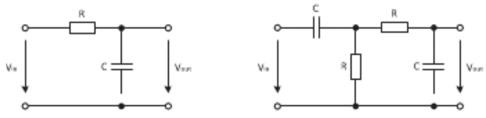
Low voltage grid topology translated into PHIL simulation system:

- MIMO ITM PIs (ITM)
  - 3-ph grid simulation
- Grid impedances (Node a/b)
  - Neutral impedances in hardware (air coils and resistances)
  - Line impedances in PHIL (VROPS)
- PV inverters
  - Single phase units (4kW, 230V/50Hz)
  - PQ control method implemented: Q(U)
  - Sourced by PV array simulators (PVAS3) in hardware

Modelling of Components

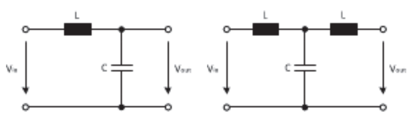
Modelling different filter designs:

- Signal Filters:
  - Used for feedback current/voltage filtering
  - By default in the system control loop
  - Examples: typically LP and BP filters
- AC Grid Filters:
  - Different Topologies used (standard literature)
  - By default connected to PHIL simulation
  - Examples: typ. Pi- or T section filters implemented
- Power Output Filters:
  - Output filter of the bridge (depending on topology)
  - Get activated during simulation (relais)
  - Examples: typ. LC or LCL filters



$$T_{LP,O1}(s) = \frac{K_1}{K_2 s + 1}.$$

$$T_{BP,O2}(s) = \frac{K_1 s}{s^2 + K_2 s + K_3}.$$



$$T_{LC}(s) = \frac{K_1}{K_2 s^2 LC + sLK_3 + K_4}.$$

Important for stability and accuracy evaluations (Nyquist)

⟶ see Viehweider A, Lauss G, Lehfuss F. *System Theoretic Aspects of Stability Determination on Linear Power Hardware-in-the-Loop Simulations*. Elsevier IJEPES-S-10-00636.

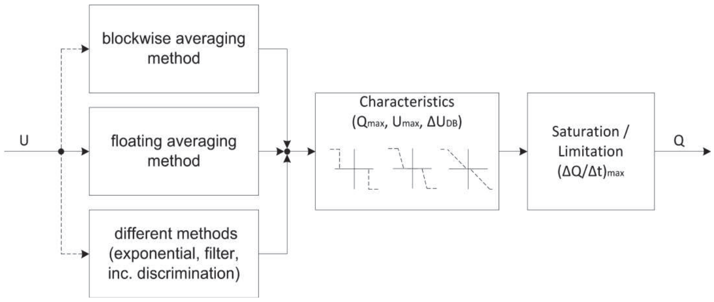
Modelling of Components

Modelling of the different PQ control methods of PV inverters:

- Fixed power factor (absolute, relative set-value)
- Cosφ(P) control
- Cosφ(U) control
- Q(U), Q(P)
- Dynamic control (free programmable)

PQ control parameter for the Q(U)-method implemented:

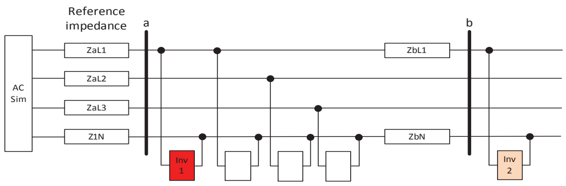
- Averaging time (grid cycles): [1; 64]
- Reactive gradient (ΔQ / Δt) [5; 200]

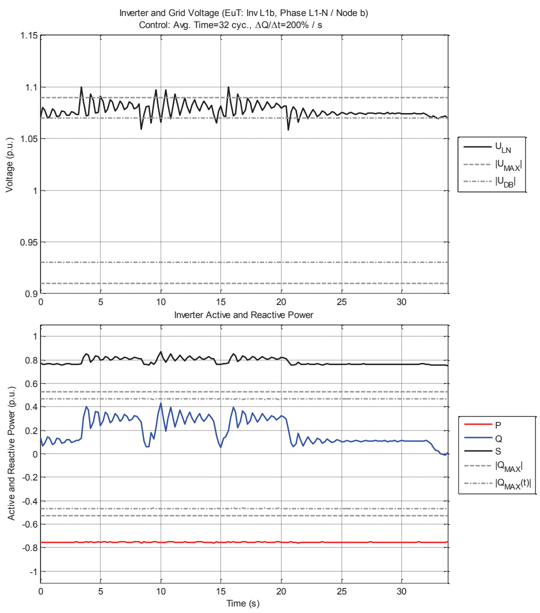


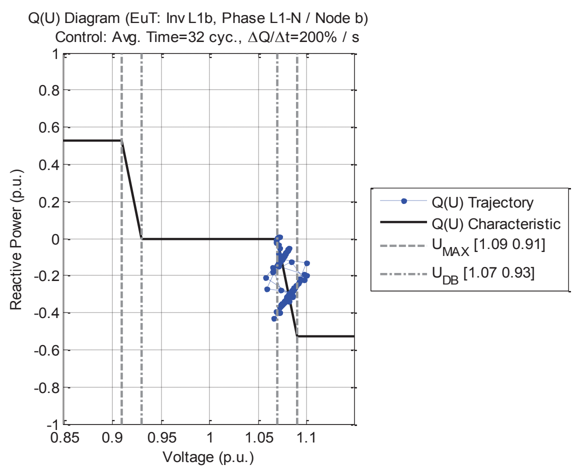
Block diagram of PQ control implementation

PQ Control Results

Use case: instabilities of PQ control (uncontrolled states)







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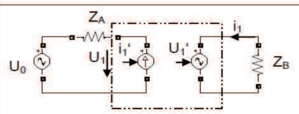
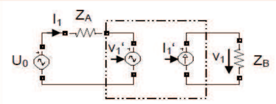
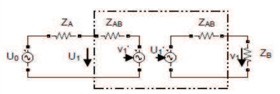
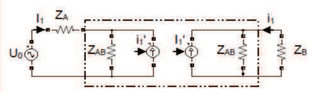
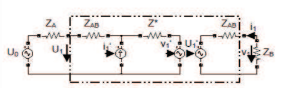
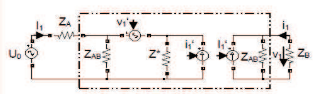
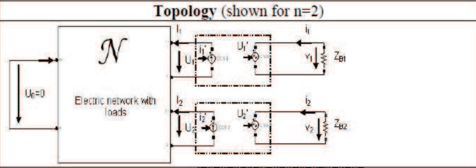
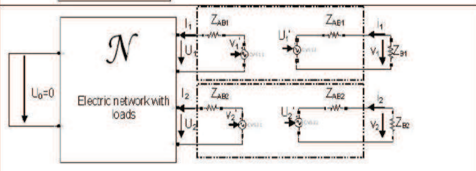
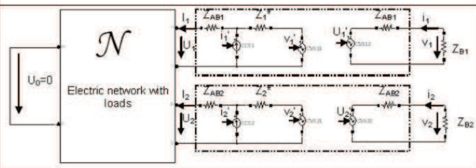
Interfacing Algorithms for PHIL

Name of the method	*Interface*	*Dual Interface (DIA)*
ITM *(Ideal Transformer Model)*	 $F_O(s)=-\frac{Z_A(s)}{Z_B(s)}e^{-sT_S}T_{VA}(s)T_C(s)$	 $F_O(s)=-\frac{Z_B(s)}{Z_A(s)}e^{-sT_S}T_{CA}(s)T_V(s)$
PCD *(Partial Circuit Duplication)*	 $F_O(s)=\frac{Z_A(s)Z_B(s)}{(Z_A(s)+Z_{AB}(s))(Z_B(s)+Z_{AB}(s))}e^{-sT_S}T_{VA}(s)T_V(s)$	 $F_O(s)=\frac{Z_{AB}^2(s)}{(Z_A(s)+Z_{AB}(s))(Z_B(s)+Z_{AB}(s))}e^{-sT_S}T_{CA}(s)T_C(s)$
DIM *(Damping Impedance Method)*	 $F_O(s)=\frac{Z_A(s)(T_V(s)Z_B(s)-T_C(s)Z^*(s))}{(Z_A(s)+Z^*(s)+Z_{AB}(s))(Z_B(s)+Z_{AB}(s))}e^{-sT_S}T_{VA}(s)$	 $F_O(s)=\frac{Z_{AB}^2(s)(T_C(s)Z^*(s)-T_V(s)Z_B(s))}{(Z_A(s)Z^*(s)+Z_{AB}(s)Z^*(s)+Z_A(s)Z_{AB}(s))(Z_B(s)+Z_{AB}(s))}e^{-sT_S}T_{VA}(s)$

SISO interface algorithms -Voltage & Current (DIA) Type

- ITM … current controlled voltage source (driven by the measured current at HuT)
- PCD … characterized by considering an impedance that exists on the software as well as on the hardware side of the simulation
- DIM … insertion of an additional impedance on the software side only (damping impedance)

Interfacing Algorithms for PHIL

Method	Topology (shown for n=2)	Open loop tranfer matrix
1. ITM (Ideal Transformer Model)		$\mathbf{F_O} = -\mathbf{T_C T_S T_{VA} Z_A Z_B^{-1}}$
2. PCD (Partial Circuit Duplication)		$\mathbf{F_O} = \mathbf{T_V T_S T_{VA}} * \mathbf{Z_A Z_B (Z_B + Z_{AB})(Z_A + Z_{AB})^{-1}}$
3. DIM (Damping Impedance Method)		$\mathbf{F_O} = \mathbf{T_S T_{VA}}(\mathbf{Z_A} + \mathbf{Z^*} + \mathbf{Z_{AB}})^{-1} * (\mathbf{Z_B} + \mathbf{Z_{AB}})^{-1}\mathbf{Z_A} * (\mathbf{T_V Z_B} - \mathbf{T_C Z^*})$
Key (for n=2)	$\mathbf{Z_A}$: impedance matrix of the network, $\mathbf{Z_B} = \begin{bmatrix} Z_{B1} & 0 \\ 0 & Z_{B2} \end{bmatrix}$: imp. m. of the real hardware components, $\mathbf{Z_{AB}} = \begin{bmatrix} Z_{AB1} & 0 \\ 0 & Z_{AB2} \end{bmatrix}$: imp. m. of the duplicated components, $\mathbf{Z^*} = \begin{bmatrix} Z^*_1 & 0 \\ 0 & Z^*_2 \end{bmatrix}$: imp. m. of the damping impedances, $\mathbf{T_S} = \begin{bmatrix} e^{-sT_d} & 0 \\ 0 & e^{-sT_d} \end{bmatrix}$: m. of the time delays due to sampling, $\mathbf{T_V} = \begin{bmatrix} T_{V1}(s) & 0 \\ 0 & T_{V2}(s) \end{bmatrix}$: m. of the transfer f. of the voltage probes, $\mathbf{T_C} = \begin{bmatrix} T_{C1}(s) & 0 \\ 0 & T_{C2}(s) \end{bmatrix}$: m. of the transfer f. of the current probes, $\mathbf{T_{VA}} = \begin{bmatrix} T_{VA1}(s) & 0 \\ 0 & T_{VA2}(s) \end{bmatrix}$:m. of the transfer f. of the voltage amplifiers	

MIMO interface algorithms
-Voltage & Current Type

- ITM → robust method, easy to implement (reduced accuracy)
- PCD → additional hardware necessary
- DIM → equal damping impedance on soft- and hardware side; not realistic assumption

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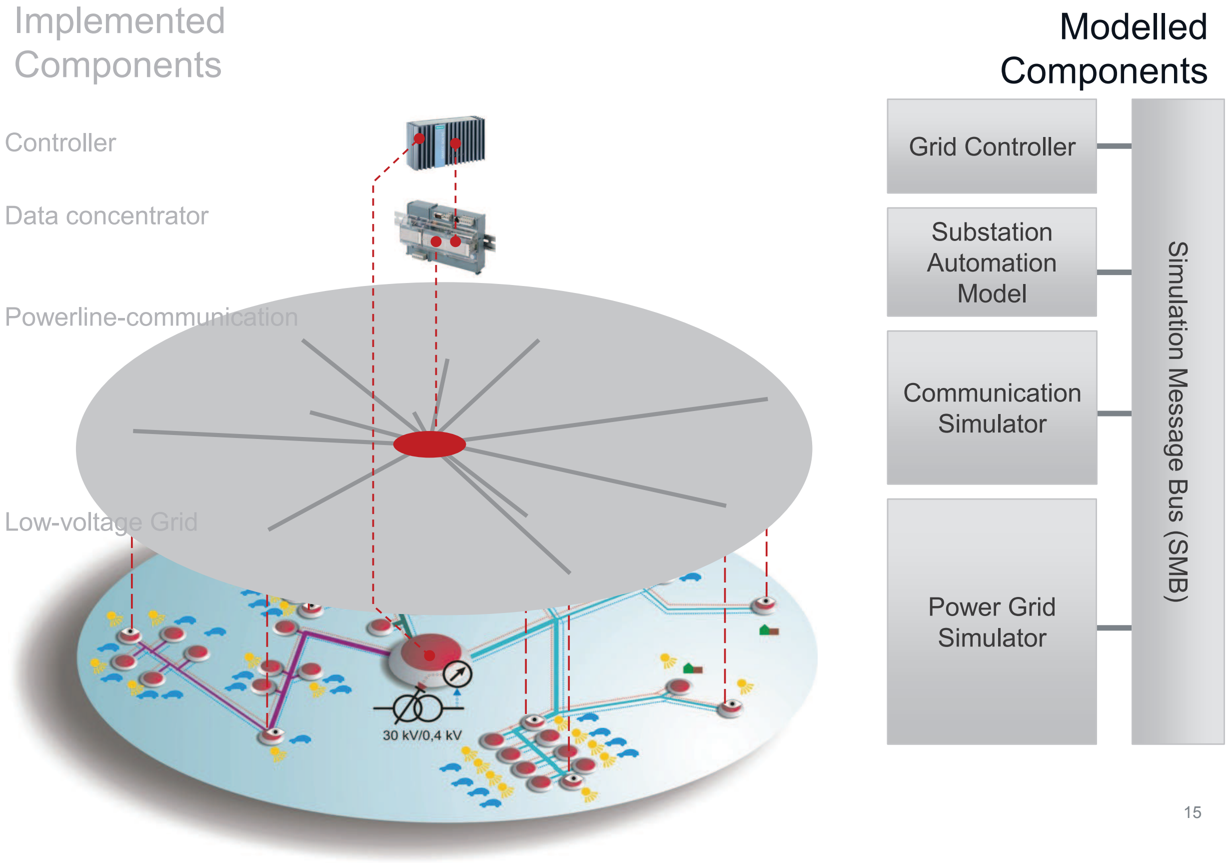
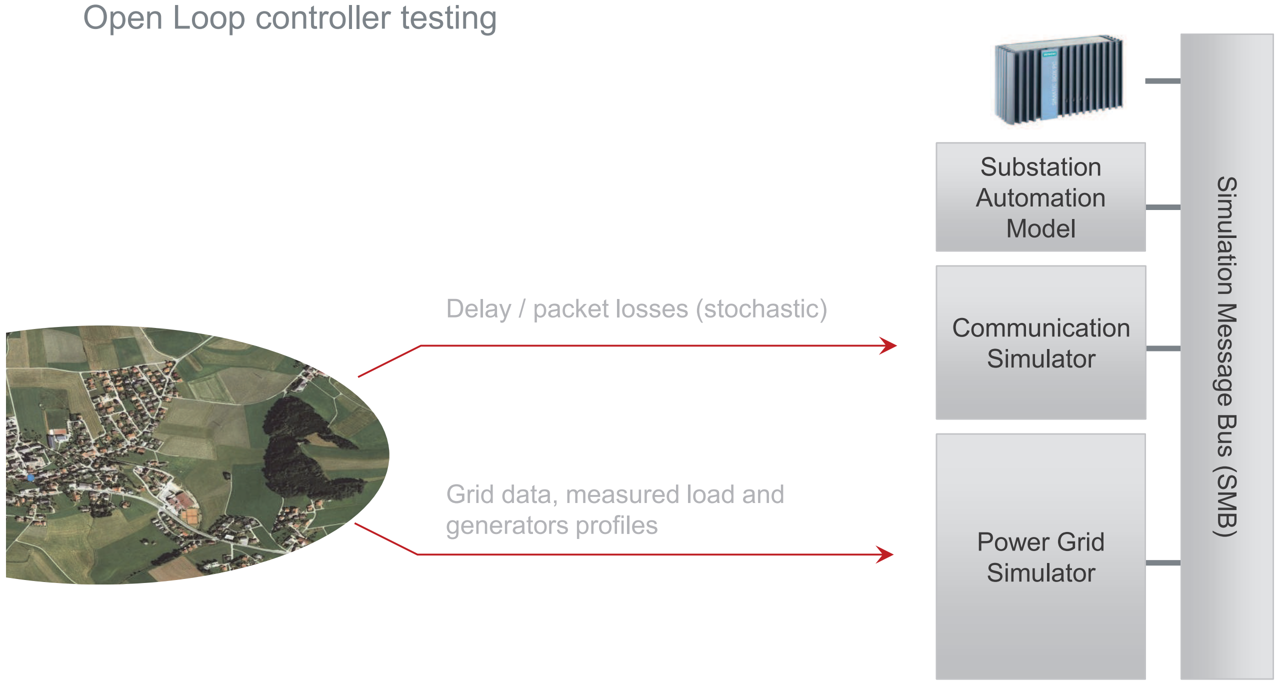
System Overview



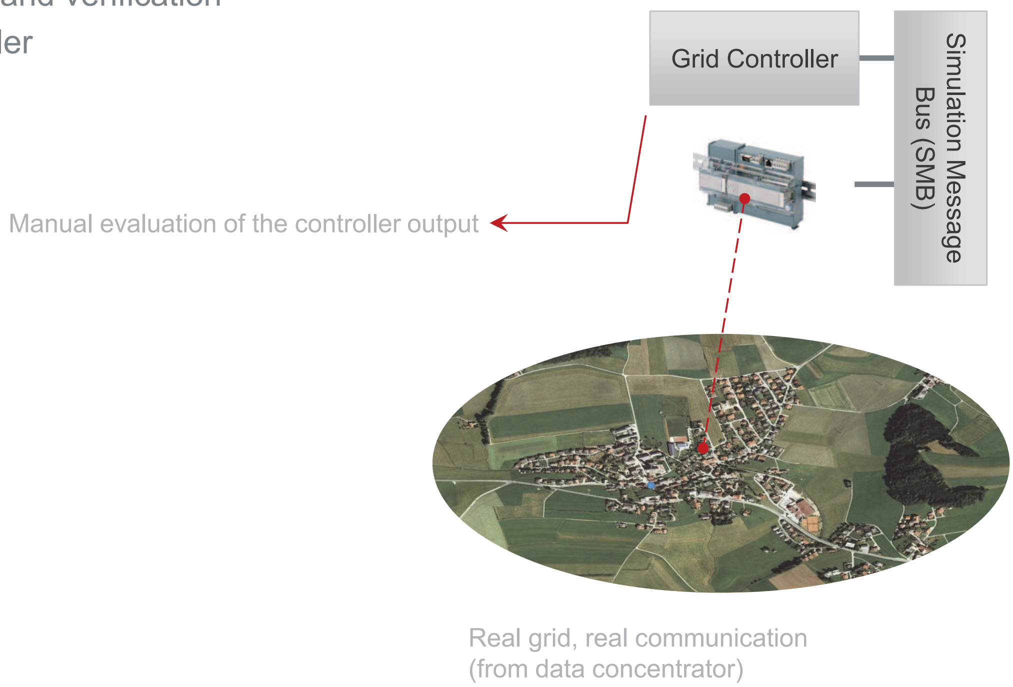
UseCase – Controller in LV Grids

Open Loop controller testing

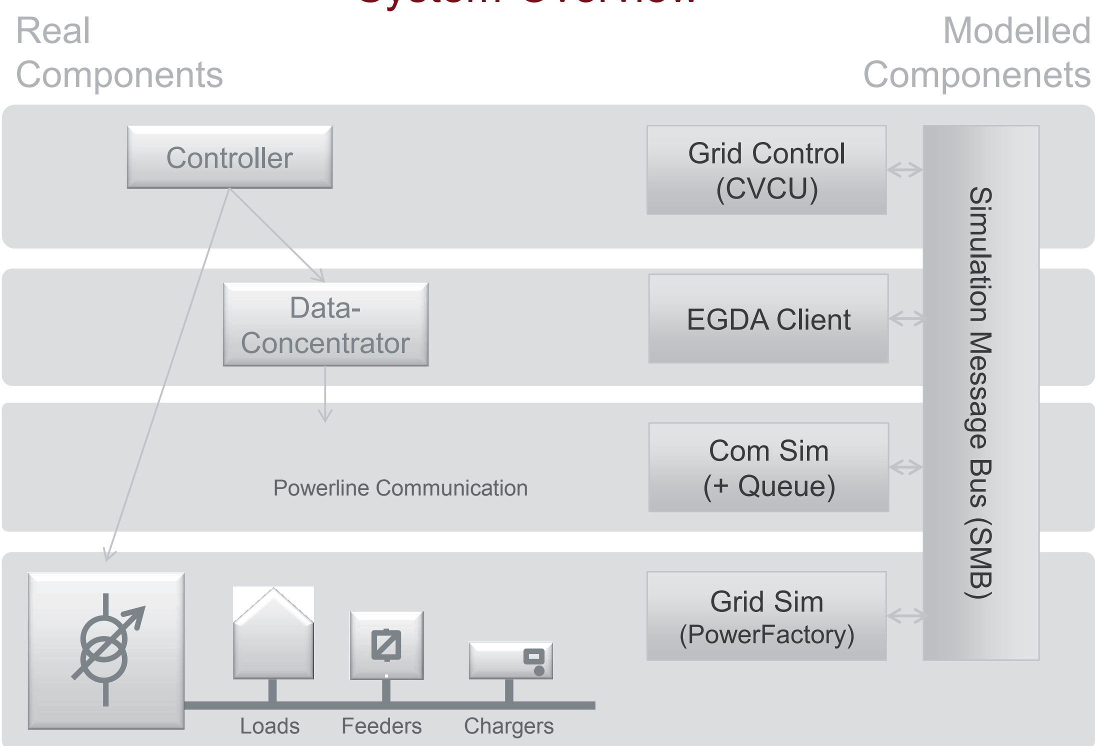


UseCase – Grid Controller

Development and verification
of grid controller

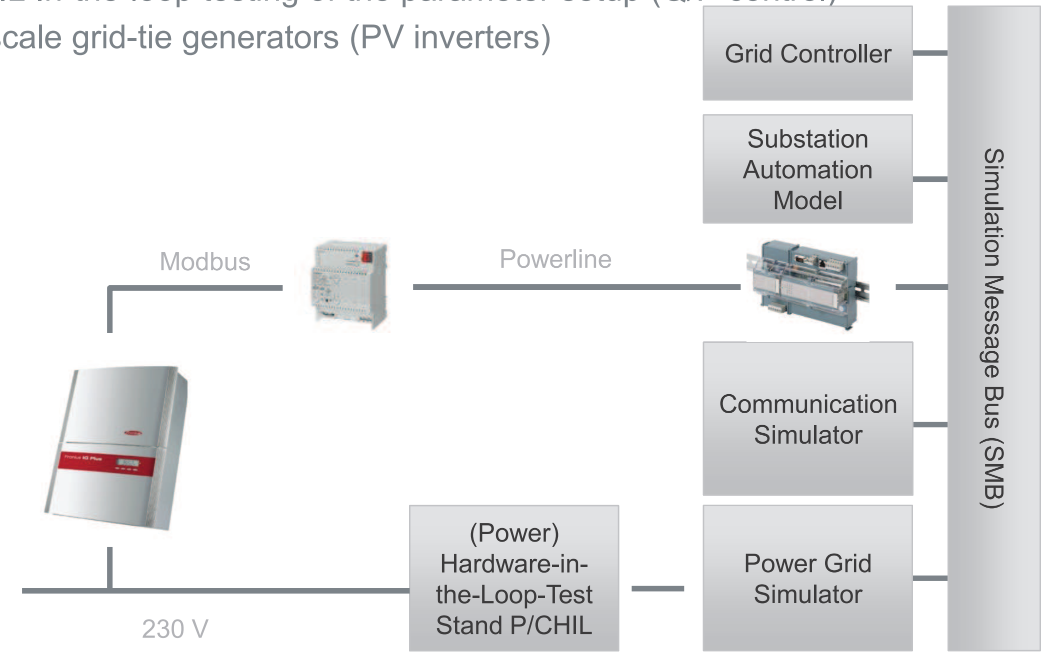


System-Overview



UseCase – (P)HIL

PHIL / CHIL In-the-loop testing of the parameter setup (Q/P control) for small-scale grid-tie generators (PV inverters)



SIMTECH laboratory - concept

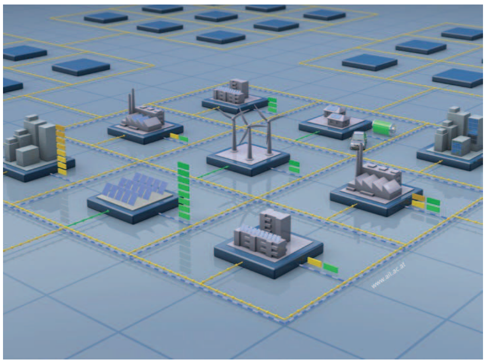
The new AIT SimTech Laboratory offers an excellent environment for testing, verification and R&D in the field of large scale DG/RES integration, and Smart Grids applications.

- DR component and systems testing with highly flexible grid and primary energy source (e.g. PV) emulation
- Electrical interconnection, functionality and performance testing according to standards
- Simultaneous testing of power and communication interfaces of DR components
- Power-Hardware-in-the-loop (PHIL) environment
- Simulation and testing of single components and whole generation systems / plants
- Emulating smart grids scenarios

AIT SimTech Laboratory
(to be inaugurated end 2012)

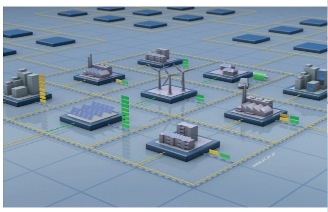
SIMTECH laboratory – electrical

- Grid simulation
  - 2 independent high bandwidth Grid Simulation Units: 0..480 V ; 3~, 800 kVA
  - 3 independent laboratory grids, which can be operated in grounded/isolated mode
  - 3-phase balanced or unbalanced operation
  - Capabilities to perform LVRT and FRT testing
- DC Sources
  - 5 independent dynamic PV-Array Simulators: 1500 V, 1500 A, 960 kVA
- Line impedance emulation
  - Adjustable line impedances for various LV network topologies: meshed, radial or ring network configuration
- Adjustable loads for active and reactive power
  - Freely adjustable RLC loads up to 1MW, 1MVAr (cap. and ind.)
  - component laboratory with highly flexible grid and primary energy source (e.g. PV) emulation (LV up to 800 kVA)
  - Parallel & serial components



SIMTECH laboratory – mechanical

- Environmental simulation
  - Test chamber for performance and accelerated lifetime testing
  - Full power operation of equipment under test inside chamber
  - Max. footprint of equipment under test: 3,60 x 2,60 x 2,80 m LxWxH
  - Temperature range -40° C..+120° C
  - Humidity range: 10%..98 % r.H.
- General Specification
  - Floor space: 400 m²
  - Indoor and Outdoor test areas suitable for ISO containers
- Power Hardware-in-the-loop (PHIL) environment
  - Multicore Opal-RT Real-Time Simulator
  - P-HIL and C-HIL experiments at full power in a closed control loop
- DAQ and Measurement
  - Multiple high precision Power Analyzers with high acquisition rate
  - Simultaneous sampling of asynchronous multi-domain data input



AIT SimTech

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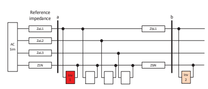
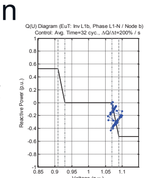
Conclusions

- Different components in single and three phase lv grids are under investigation; focus is on stability issues for active / reactive power control issues
- Nowadays, not all LV topologies can be run/translated into PHIL simulation setup; complexity of MIMO systems are challenging (stability).
- In Future, more complex lv grid scenarios should be able to be modeled and run in PHIL simulation (MIMO, advanded IA)





Outlook:

- More detailled investigations on PHIL test components (modeling) will be done in order to optimize simulation characteristics (stability, accuracy, BW, …)
- Comparison with real tests (lab, field) will give a better understanding and represents a verification.

Thank you very much for your attention!

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